REMARKS

The indication of allowable subject matter in claims 3, 6-20, 27-35, 37 and 38 is acknowledged and appreciated. Accordingly, claims 3, 6, 11, 27, 32 and 37 have been rewritten into independent form. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

As a preliminary matter, it is respectfully submitted that the objection to the drawings has been obviated by the amendment to the claims, and the title has been amended to be more descriptive.

Claims 21-26 stand rejected under 35 U.S.C. § 112, first paragraph (enablement). It is respectfully submitted that the enclosed amendment obviates this rejection, support for which can be found on page 23, line 17+ of Applicant's specification corresponding to Figure 11 of Applicant's drawings.

Claims 1, 2, 4, 5 and 36 stand rejected under 35 U.S.C. § 102 as being anticipated by Saito et al.. Claim 1 is independent. This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "a timing adjustment circuit block provided ***between*** the first and second circuit blocks for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other" (emphasis added). In contrast, as shown in Figure 4 of Saito et al., the alleged timing adjustment circuits 406,407 are provided ***inside*** the logic circuit block 402. Accordingly, the logic circuit blocks of Saito et al.

are subject to having an increased size for providing additional area for containing the timing circuits therein.

Moreover, according to one aspect of the present invention as now recited in claim 1, it is possible to place the timing adjustment circuit on a line between the first and second circuit blocks even after placement of the first/second circuit blocks completes the system LSI. In this regard, the present invention further enables placement of the timing adjustment circuit in the dead space created after the placement of the reduced-size logic circuit blocks in the system LSI, thereby further minimizing size by reducing wasted space and optimizing efficient use of space.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Saito et al. does not anticipate the independent claims, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

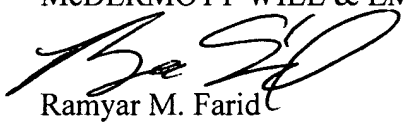
CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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